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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/626,420	SHANTZ ET AL.
	Examiner	Art Unit
	Carlton V. Johnson	2136

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 02 July 2007.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-65 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-65 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO/SB/08)
 Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
 5) Notice of Informal Patent Application
 6) Other: _____

DETAILED ACTION

1. This action is responding to application papers filed on **7-2-2007**.
2. Claims **1 - 65** are pending. Claims **1, 4, 5, 6, 7, 10, 12, 13, 14, 16, 18, 22, 23, 24, 25, 27, 29, 31, 32, 36, 38, 41, 43, 44, 47, 50, 51, 53, 53, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65** have amended. Claims **1, 18, 43, 50, 57, 61, 64, 65** are independent.

Response to Arguments

3. Applicant's arguments filed 7/2/2007 have been fully considered but they are not persuasive.
- 3.1 Applicant argues that the referenced prior art does not disclose, "*adding implicitly a partial result from a previously executed single arithmetic instruction to generate a result that represents the first number multiplied by the second number summed with the partial result*". (see Remarks Pages 17, 19)

The Gressel prior art disclose arithmetic operations such as multiplication and addition utilizing the partial results of the first operation. (see Gressel col. 3, lines 1-7; col. 53, lines 13-19; col. 53, lines 49-51: feedback of a previous operation into next operation; col. 2, lines 31-37: multiplication two values, summing two values utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results from previous multiplication)

In very long instruction word (VLIW) architectures, which include many microcode architectures, multiple simultaneous operations and operands are specified in a single

instruction. (<http://www.answers.com/topic/instruction-computer-science>) This standard computer architecture feature discloses a single arithmetic instruction to perform multiple operations.

An instruction also designates the destination address (memory locations, registers) for the results of the completion of an instruction. (*"On traditional architectures, an instruction includes an opcode specifying the operation to be performed, such as "add contents of memory to register", and zero or more operand specifiers, which may specify registers, memory locations, or literal data "*:
<http://www.answers.com/topic/instruction-computer-science>)

3.2 Applicant argues that the referenced prior art does not disclose, *"a high order portion of a result of the previously executed single arithmetic instruction "*. (see Remarks Page 18)

The Gressel prior art discloses partial results from an arithmetic operation. The partial results could be the high order bits. (see Gressel col. 2, lines 31-37: arithmetic operations utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results from previous multiplication)

3.3 Applicant argues that the referenced prior art does not disclose, *"storing at least a portion of the generated result; and using the stored at least a portion of the generated result in a subsequent computation in a cryptography application"*. (see Remarks Page 18)

The Gressel prior art discloses storing and utilizing the results of an operation in subsequent arithmetic operations. (see Gressel col. 3, lines 1-7; col. 53, lines 13-19; col. 53, lines 49-51: feedback of a previous operation into a next (subsequent) operation)

3.4 The examiner has considered the applicant's remarks concerning a cryptographic application executing arithmetic instructions; a first number is multiplied by a second number, and a partial result from a previously executed arithmetic instruction is added to generate a result that represents the first number multiplied by the second number summed with the partial result from a previously executed single arithmetic instruction; the high order portion of the generated result is saved in an extended carry register as a next partial result for use with execution of a subsequent single arithmetic instruction. Applicant's arguments have thus been fully analyzed and considered but they are not persuasive.

After an additional analysis of the applicant's invention, remarks, and a search of the available prior art, it was determined that the current set of prior art consisting of Gressel (6,748,410) and Stribaek (7,181,484) discloses the applicant's invention including disclosures in Remarks dated July 2, 2007.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 1 - 65 are rejected under 35 U.S.C. 101 because the claimed invention is based on non-statutory subject matter and directed towards nothing more than the abstract idea of a mathematical algorithm. Abstract ideas are not eligible for patent protection. A claimed invention reciting a computer program product that solely calculates a mathematical formula or a computer readable medium that solely stores a mathematical formula is not directed to the type of subject matter eligible for patent protection.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1 - 5, 13 - 23, 30, 33 - 46, 49 - 52, 56 - 65 are rejected under 35 U.S.C. 102(e) as being anticipated by **Gressel et al.** (US Patent No. 6,748,410).

Regarding Claim 1, Gressel discloses a method implemented in a device supporting a cryptography application, the method comprising: in response to executing a single arithmetic instruction, multiplying a first number by a second number; and adding implicitly a partial result from a previously executed single arithmetic instruction to

generate a result that represents the first number multiplied by the second number summed with the partial result, wherein the partial result comprises a high order portion of a result of the previously executed single arithmetic instruction; storing at least a portion of the generated result; and using the stored at least a portion of the generated result in a subsequent computation in the cryptography application. (see Gressel col. 3, lines 1-7; col. 53, lines 13-19; col. 53, lines 49-51: feedback of a previous operation into next operation; col. 3, lines 28-32; col. 11, lines 7-11; col. 11, lines 40-49: arithmetic operation or instructions; col. 31, lines 44-46; col. 41, lines 3-5: arithmetic structure; col. 2, lines 31-37: multiplication two values, summing two values utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results from previous multiplication; col. 6, lines 20-25: adder; col. 2, lines 4-9; col. 5, lines 58-67; col. 41, lines 20-23: register usage; col. 8, lines 59-60; col. 53, lines 13-19: XOR operations; col. 29, lines 43-49: redundant representation of numbers; col. 1, lines 39-45; col. 5, lines 23-25: acceleration, improvements of arithmetic operations; col. 3, lines 28-32: arithmetic operations utilized to generate cryptographic key(s); col. 3, lines 18-22: processor utilization for key generation)

Regarding Claim 2, Gressel discloses the method as recited in claim 1 further comprising performing the adding of the partial result as part of addition operations performed for the multiplying of the first and second number. (see Gressel col. 2, lines 31-37: multiplication two values, summing two values utilizing partial (i.e. bit operations,

any bit length, high order bits, low order bits) results from previous multiplication)

Regarding Claim 3, Gressel discloses the method as recited in claim 1 wherein the partial result is in redundant number representation. (see Gressel col. 29, lines 43-49: redundant representation of numbers)

Regarding Claim 4, Gressel discloses the method as recited in claim 1, wherein said adding the partial result comprises adding the partial result to a multiplication result of the first and second numbers. (see Gressel col. 2, lines 31-37: multiplication two values, summing two values utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results from previous multiplication)

Regarding Claim 5, Gressel discloses the method as recited in claim 1, wherein said storing at least a portion of the generated result comprises storing a high order portion of the generated result as a next partial result for use with execution of a subsequent single arithmetic instruction. (see Gressel col. 3, lines 1-7; col. 53, lines 13-19; col. 53, lines 49-51: feedback of a previous operation into next operation)

Regarding Claim 13, Gressel discloses the method as recited in claim 1, wherein the single arithmetic instruction is a single multiply-accumulate instruction; wherein the first and second numbers are specified in the single multiply-accumulate instruction as first and second source registers and a low order portion of the result is stored in a

destination location specified in the single multiply-accumulate instruction. (see Gressel col. 3, lines 28-32; col. 11, lines 7-11; col. 11, lines 40-49: arithmetic operation or instructions; col. 3, lines 1-7; col. 53, lines 13-19; col. 53, lines 49-51: feedback of a previous operation into next operation)

Regarding Claim 14, Gressel discloses the method as recited in claim 5 wherein the first and second numbers are n-bit numbers, n being a positive integer and wherein the high order portion of the generated result is an n-bit portion. (see Gressel col. 2, lines 31-37: arithmetic operations utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results from previous operations)

Regarding Claim 15, Gressel discloses the method as recited in claim 5 further comprising: in response to executing the subsequent single arithmetic instruction, multiplying third and fourth numbers specified by the subsequent single arithmetic instruction and adding implicitly the next partial result to generate a second result that represents the third number multiplied by the fourth number summed with the next partial result. (see Gressel col. 3, lines 28-32; col. 11, lines 7-11; col. 11, lines 40-49: arithmetic operation or instructions; col. 2, lines 31-37: multiplication two values, summing two values utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results from previous multiplication)

Regarding Claim 16, Gressel discloses the method as recited in claim 15, further

comprising storing the high order portion of the second result to be implicitly added in response to executing another subsequent single arithmetic instruction. (see Gressel col. 3, lines 1-7; col. 53, lines 13-19; col. 53, lines 49-51: feedback of a previous operation into next operation; col. 2, lines 31-37: arithmetic operations utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results from previous opeeration)

Regarding Claim 17, Gressel discloses the method as recited in claim 1 wherein the multiplying and adding are implemented to support XOR operations for binary polynomial fields. (see Gressel col. 8, lines 59-60; col. 53, lines 13-19: XOR operations)

Regarding Claim 18, Gressel discloses a method implemented in a device supporting a cryptography application, the method comprising: in response to executing a single arithmetic instruction, multiplying a first number by a second number; adding implicitly a partial result from a previously executed single arithmetic instruction, wherein the partial result comprises a high order porution of a result of the previously executed single arithmetic instruction; adding a third number to generate a result that represents the first number multiplied by the second number summed with the partial result and the third number; storing at least a portion of the generated result; and using the stored at least a portion of the generated result in a subsequent computation in the cryptography application. (see Gressel col. 3, lines 1-7; col. 53, lines 13-19; col. 53, lines 49-51: feedback of a previous operation into next operation; col. 3, lines 28-32; col. 11, lines

7-11; col. 11, lines 40-49: arithmetic operation or instructions; col. 31, lines 44-46; col. 41, lines 3-5: arithmetic structure; col. 2, lines 31-37: multiplication two values, summing two values utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results from previous multiplication; col. 6, lines 20-25: adder; col. 2, lines 4-9; col. 5, lines 58-67; col. 41, lines 20-23: register usage; col. 8, lines 59-60; col. 53, lines 13-19: XOR operations; col. 29, lines 43-49: redundant representation of numbers; col. 1, lines 39-45; col. 5, lines 23-25: acceleration, improvements of arithmetic operations; col. 3, lines 28-32: arithmetic operations utilized to generate cryptographic key(s); col. 3, lines 18-22: processor utilization for key generation)

Regarding Claim 19, Gressel discloses the method as recited in claim 18 further comprising performing the adding of the partial result as part of addition performed for the multiplying of the first and second number. (see Gressel col. 2, lines 31-37: multiplication two values, summing two values utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results from previous multiplication)

Regarding Claim 20, Gressel discloses the method as recited in claim 18 wherein the partial result is stored in a redundant number representation. (see Gressel col. 29, lines 43-49: redundant representation of numbers)

Regarding Claim 21, Gressel discloses the method as recited in claim 18 further comprising performing the adding of the third number as part of the addition performed

for the multiplying of the first and second number. (see Gressel col. 2, lines 31-37: multiplication two values, summing two values utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results from previous multiplication)

Regarding Claim 22, Gressel discloses the method as recited in claim 18, wherein said adding the partial result comprises adding the partial result after generation of a multiplication result of multiplying the first and second numbers. (see Gressel col. 2, lines 31-37: multiplication two values, summing two values utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results from previous multiplication)

Regarding Claim 23, Gressel discloses the method as recited in claim 18, wherein said storing at least a portion of the generated result comprises storing a high order portion of the generated result as a next partial multiplication result for use with execution of a subsequent single arithmetic instruction. (see Gressel col. 3, lines 1-7; col. 53, lines 13-19; col. 53, lines 49-51: feedback of a previous operation into next operation; col. 2, lines 31-37: multiplication two values, summing two values utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results from previous multiplication)

Regarding Claim 30, Gressel discloses the method as recited in claim 24 wherein the second number is implicitly identified in the single arithmetic instruction. (see Gressel

col. 3, lines 28-32; col. 11, lines 7-11; col. 11, lines 40-49: arithmetic operation or instructions: long instruction word, multiple instructions)

Regarding Claim 33, Gressel discloses the method as recited in claim 18 wherein the first and third numbers are specified in the single arithmetic instruction as first and second source registers and a low order portion of the generated result is stored in a destination location specified in the single arithmetic instruction. (see Gressel col. 3, lines 28-32; col. 11, lines 7-11; col. 11, lines 40-49: arithmetic operation or instructions)

Regarding Claim 34, Gressel discloses the method as recited in claim 33 wherein the partial result from a previously executed single arithmetic instruction is implicitly specified by the single arithmetic instruction and wherein the second number is explicitly specified by a third source register in the single arithmetic instruction. (see Gressel col. 3, lines 28-32; col. 11, lines 7-11; col. 11, lines 40-49: arithmetic operation or instructions)

Regarding Claim 35, Gressel discloses the method as recited in claim 33 wherein the partial result from a previously executed single arithmetic instruction is implicitly specified by the single arithmetic instruction and the second number is implicitly specified by the single arithmetic instruction. (see Gressel col. 3, lines 28-32; col. 11, lines 7-11; col. 11, lines 40-49: arithmetic operation or instructions)

Regarding Claim 36, Gressel discloses the method as recited in claim 23 further comprising: in response to executing the subsequent single arithmetic instruction, multiplying a fourth number and a fifth number, the fourth number being specified by the subsequent single arithmetic instruction, adding implicitly the next partial multiplication result and adding a sixth number to generate a second result, the second result representing the fourth number multiplied by the fifth number summed with the next partial result and the sixth number. (see Gressel col. 3, lines 28-32; col. 11, lines 7-11; col. 11, lines 40-49: arithmetic operation or instructions)

Regarding Claim 37, Gressel discloses the method as recited in claim 36 wherein the fifth number and the second number are equal. (see Gressel col. 29, lines 43-49: representation of numbers)

Regarding Claim 38, Gressel discloses the method as recited in claim 36 further comprising storing a high order portion of the second result to be implicitly added in response to executing another subsequent single arithmetic instruction. (see Gressel col. 3, lines 1-7; col. 53, lines 13-19; col. 53, lines 49-51: feedback of a previous operation into next operation; col. 2, lines 31-37: arithmetic operations utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results from previous multiplication)

Regarding Claim 39, Gressel discloses the method as recited in claim 18 wherein the

first number is specified in the single arithmetic instruction in a first source register, the second number is contained in a special register and is not specified in the single arithmetic instruction, the third number is specified as a second source register in the single arithmetic instruction and a low order portion of the generated result is stored in a destination location specified in the single arithmetic instruction. (see Gressel col. 3, lines 28-32; col. 11, lines 7-11; col. 11, lines 40-49: arithmetic operation or instructions)

Regarding Claim 40, Gressel discloses the method as recited in claim 18 wherein the first, second, and third numbers are specified by source operands in the single arithmetic instruction. (see Gressel col. 3, lines 28-32; col. 11, lines 7-11; col. 11, lines 40-49: arithmetic operation or instructions)

Regarding Claim 41, Gressel discloses the method as recited in claim 18 wherein a destination location and one of the first number, the second number, and the third number are specified by one operand in the single arithmetic instruction. (see Gressel col. 3, lines 28-32; col. 11, lines 7-11; col. 11, lines 40-49: arithmetic operation or instructions)

Regarding Claim 42, Gressel discloses the method as recited in claim 18 wherein the multiplying and adding operations are implemented for binary polynomial fields. (see Gressel col. 2, lines 31-37: multiplication two values, summing two values utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results from

previous multiplication; col. 6, lines 20-25: adder; col. 31, lines 46-48; col. 6, line 66 - col. 7, line 9; col. 31, lines 44-46: carry-save adder; multiplying and adding operations)

Regarding Claim 43, Gressel discloses a processor comprising an arithmetic circuit, the processor configured to be responsive to execution of a single arithmetic instruction to cause the arithmetic circuit to multiply a first number and a second number and to add implicitly a high order portion of a partial result from a previously executed single arithmetic instruction, thereby generating a result that represents the first number multiplied by the second number summed with the high order portion of the partial result; store at least a portion of the generated result; and use the stored at least a portion of the generated result in a subsequent computation. (see Gressel col. 3, lines 1-7; col. 53, lines 13-19; col. 53, lines 49-51: feedback of a previous operation into next operation; col. 3, lines 28-32; col. 11, lines 7-11; col. 11, lines 40-49: arithmetic operation or instructions; col. 31, lines 44-46; col. 41, lines 3-5: arithmetic structure; col. 2, lines 31-37: multiplication two values, summing two values utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results from previous multiplication; col. 6, lines 20-25: adder; col. 2, lines 4-9; col. 5, lines 58-67; col. 41, lines 20-23: register usage; col. 8, lines 59-60; col. 53, lines 13-19: XOR operations; col. 29, lines 43-49: redundant representation of numbers; col. 1, lines 39-45; col. 5, lines 23-25: acceleration, improvements of arithmetic operations; col. 3, lines 28-32: arithmetic operations utilized to generate cryptographic key(s); col. 3, lines 18-22:

processor utilization for key generation)

Regarding Claim 44, Gressel discloses the processor as recited in claim 43, wherein to store at least a portion of the generated result, the processor is further responsive to the single arithmetic instruction to store a high order portion of the generated result into an extended carry register for use with execution of a subsequent single arithmetic instruction. (see Gressel col. 3, lines 28-32; col. 11, lines 7-11; col. 11, lines 40-49: arithmetic operation or instructions)

Regarding Claim 45, Gressel discloses the processor as recited in claim 43 wherein the high order portion of the previously executed single arithmetic instruction is stored in a redundant number representation. (see Gressel col. 3, lines 28-32; col. 11, lines 7-11; col. 11, lines 40-49: arithmetic operation or instructions; col. 29, lines 43-49: redundant representation of numbers)

Regarding Claim 46, Gressel discloses the processor as recited in claim 45, wherein the extended carry register is a register accessible via a processor instruction. (see Gressel col. 3, lines 28-32; col. 11, lines 7-11; col. 11, lines 40-49: arithmetic operation or instructions) (see Stribaek col. 5, lines 41-45: extended carry operations)

Regarding Claim 49, Gressel discloses the processor as recited in claim 43 wherein the first and second numbers are specified in the single arithmetic instruction as first

and second source registers. (see Gressel col. 3, lines 28-32; col. 11, lines 7-11; col. 11, lines 40-49: arithmetic operation or instructions)

Regarding Claim 50, Gressel discloses a processor comprising an arithmetic circuit, the processor configured to be responsive to execution of a single arithmetic instruction to: cause the arithmetic circuit to multiply a first number and a second number to add a third number and to implicitly add a high order portion of a previous result from a previously executed single arithmetic instruction thereby generating a result that represents the first number multiplied with the second number, summed with the high order portion of the previous result and with the third number; store at least a portion of the generated result; and use the stored at least a portion of the generated result in a subsequent computation. (see Gressel col. 3, lines 1-7; col. 53, lines 13-19; col. 53, lines 49-51: feedback of a previous operation into next operation; col. 3, lines 28-32; col. 11, lines 7-11; col. 11, lines 40-49: arithmetic operation or instructions; col. 31, lines 44-46; col. 41, lines 3-5: arithmetic structure; col. 2, lines 31-37: multiplication two values, summing two values utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results from previous multiplication; col. 6, lines 20-25: adder; col. 2, lines 4-9; col. 5, lines 58-67; col. 41, lines 20-23: register usage; col. 8, lines 59-60; col. 53, lines 13-19: XOR operations; col. 29, lines 43-49: redundant representation of numbers; col. 1, lines 39-45; col. 5, lines 23-25: acceleration, improvements of arithmetic operations; col. 3, lines 28-32: arithmetic operations utilized

to generate cryptographic key(s); col. 3, lines 18-22: processor utilization for key generation)

Regarding Claim 51, Gressel discloses the processor as recited in claim 50 wherein to store at least a portion of the generated result, the processor is configured to store a high order portion of the generated result for use with execution of a subsequent single arithmetic instruction. (see Gressel col. 2, lines 31-37: arithmetic operations utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results)

Regarding Claim 52, Gressel discloses the processor as recited in claim 50 wherein the high order portion of the previous result is stored in a redundant number representation. (see Gressel col. 2, lines 31-37: arithmetic operations utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results; col. 29, lines 43-49: redundant representation of numbers)

Regarding Claim 56, Gressel discloses the processor as recited in claim 50, wherein the first number is specified in the single arithmetic instruction as a first source register, the second number is contained in a logically local register and is not specified in the single arithmetic instruction, the third number is specified as a second source register in the single arithmetic instruction and a low order portion of the result is stored in a destination location specified in the single arithmetic instruction. (see Gressel col. 3, lines 28-32; col. 11, lines 7-11; col. 11, lines 40-49: arithmetic operation or instructions)

Regarding Claim 57, Gressel discloses a computer-readable storage medium, comprising program instructions executable by a processor to implement a cryptography application: wherein a single arithmetic instruction in the cryptography application causes the processor to multiply a first number by a second number and to implicitly add a high order portion of a previously executed single arithmetic instruction to generate a result that represents the first number multiplied with the second number and summed with the high order portion of a previously executed single arithmetic instruction, wherein the single arithmetic instruction further causes the processor to store a high order portion of the generated result for use with execution of a subsequent single arithmetic instruction in the cryptography application. (see Gressel col. 3, lines 1-7; col. 53, lines 13-19; col. 53, lines 49-51: feedback of a previous operation into next operation; col. 3, lines 28-32; col. 11, lines 7-11; col. 11, lines 40-49: arithmetic operation or instructions; col. 31, lines 44-46; col. 41, lines 3-5: arithmetic structure; col. 2, lines 31-37: multiplication two values, summing two values utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results from previous multiplication; col. 6, lines 20-25: adder; col. 2, lines 4-9; col. 5, lines 58-67; col. 41, lines 20-23: register usage; col. 8, lines 59-60; col. 53, lines 13-19: XOR operations; col. 29, lines 43-49: redundant representation of numbers; col. 1, lines 39-45; col. 5, lines 23-25: acceleration, improvements of arithmetic operations; col. 3, lines 28-32: arithmetic operations utilized to generate cryptographic key(s); col. 3, lines 18-22: processor utilization for key generation)

Regarding Claim 58, Gressel discloses the storage medium as recited in claim 57 wherein the single arithmetic instruction includes a first source operand and a second source operand, specifying the first number and the second number, and a destination operand wherein the single arithmetic instruction further causes the processor to store a low order portion of the generated result in a location specified by the destination operand. (see Gressel col. 2, lines 31-37: arithmetic operations utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results)

Regarding Claim 59, Gressel discloses the storage medium as recited in claim 57, wherein the subsequent single arithmetic instruction causes the processor executing the subsequent single arithmetic instruction to multiply a third number by a fourth number and implicitly add the high order portion of the result. (see Gressel col. 2, lines 31-37: multiplication two values, summing two values utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results from previous multiplication)

Regarding Claim 60, Gressel discloses the storage medium as recited in claim 59, wherein another single arithmetic instruction in the cryptography application causes the processor to multiply a fifth number by a sixth number and to generate another result without implicitly adding another high order portion of another previously executed result and to store a high order portion of the other result for use with another subsequent

single arithmetic instruction. (see Gressel col. 3, lines 28-32; col. 11, lines 7-11; col. 11, lines 40-49: arithmetic operation or instructions)

Regarding Claim 61, Gressel discloses a computer-readable storage medium, comprising program instructions executable by a processor to implement a cryptography application: wherein a single arithmetic instruction in the cryptography application causes the processor to: multiply a first number by a second number; add implicitly a partial multiplication result from a previously executed single arithmetic instruction and a third number to generate a result that represents the first number multiplied by the second number summed with the partial multiplication result and summed with the third number; and store a high order portion of the generated result for use with execution of a subsequent single arithmetic instruction in the cryptography application. (see Gressel col. 3, lines 1-7; col. 53, lines 13-19; col. 53, lines 49-51: feedback of a previous operation into next operation; col. 3, lines 28-32; col. 11, lines 7-11; col. 11, lines 40-49: arithmetic operation or instructions; col. 31, lines 44-46; col. 41, lines 3-5: arithmetic structure; col. 2, lines 31-37: multiplication two values, summing two values utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results from previous multiplication; col. 6, lines 20-25: adder; col. 2, lines 4-9; col. 5, lines 58-67; col. 41, lines 20-23: register usage; col. 8, lines 59-60; col. 53, lines 13-19: XOR operations; col. 29, lines 43-49: redundant representation of numbers; col. 1, lines 39-45; col. 5, lines 23-25: acceleration, improvements of

arithmetic operations; col. 3, lines 28-32: arithmetic operations utilized to generate cryptographic key(s); col. 3, lines 18-22: processor utilization for key generation)

Regarding Claim 62, Gressel discloses the storage medium as recited in claim 61, wherein the subsequent second single arithmetic instruction causes the processor to multiply a fourth number by the second number to add a fifth number, and to implicitly add the high order portion of the generated result. (see Gressel col. 2, lines 31-37: multiplication two values, summing two values utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results from previous multiplication)

Regarding Claim 63, Gressel discloses the storage medium as recited in claim 61, wherein the subsequent single arithmetic instruction causes the processor to multiply a fourth number by a fifth number, to add a sixth number, and to implicitly add the high order portion of the result. (see Gressel col. 2, lines 31-37: multiplication two values, summing two values utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results from previous multiplication)

Regarding Claim 64, Gressel discloses a processor supporting a cryptography application comprising: means, responsive to a single multiply-accumulate instruction in the cryptography application, for multiplying a first number with a second number and implicitly adding a partial result of a previously executed single multiply-accumulate instruction to generate a result that represents the first number multiplied by the second

number summed with the partial result; and means for storing a high order portion of the result for use with execution of a subsequent single multiply-accumulate instruction in the cryptography application. (see Gressel col. 3, lines 1-7; col. 53, lines 13-19; col. 53, lines 49-51: feedback of a previous operation into next operation; col. 3, lines 28-32; col. 11, lines 7-11; col. 11, lines 40-49: arithmetic operation or instructions; col. 31, lines 44-46; col. 41, lines 3-5: arithmetic structure; col. 2, lines 31-37: multiplication two values, summing two values utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results from previous multiplication; col. 6, lines 20-25: adder; col. 2, lines 4-9; col. 5, lines 58-67; col. 41, lines 20-23: register usage; col. 8, lines 59-60; col. 53, lines 13-19: XOR operations; col. 29, lines 43-49: redundant representation of numbers; col. 1, lines 39-45; col. 5, lines 23-25: acceleration, improvements of arithmetic operations; col. 3, lines 28-32: arithmetic operations utilized to generate cryptographic key(s); col. 3, lines 18-22: processor utilization for key generation)

Regarding Claim 65, Gressel discloses a processor supporting a cryptography application, comprising: means, responsive to a single multiply-accumulate instruction in a cryptography application, for multiplying a first number with a second number, for implicitly adding a partial result of a previously executed single multiply-accumulate instruction, and for adding a third number to generate a result that represents the first number multiplied by the second number summed with the partial result and the third number; and means for storing a high order portion of the generated result for use with

execution of a subsequent multiply-accumulate instruction in the cryptography application. (see Gressel col. 3, lines 1-7; col. 53, lines 13-19; col. 53, lines 49-51: feedback of a previous operation into next operation; col. 3, lines 28-32; col. 11, lines 7-11; col. 11, lines 40-49: arithmetic operation or instructions; col. 31, lines 44-46; col. 41, lines 3-5: arithmetic structure; col. 2, lines 31-37: multiplication two values, summing two values utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results from previous multiplication; col. 6, lines 20-25: adder; col. 2, lines 4-9; col. 5, lines 58-67; col. 41, lines 20-23: register usage; col. 8, lines 59-60; col. 53, lines 13-19: XOR operations; col. 29, lines 43-49: redundant representation of numbers; col. 1, lines 39-45; col. 5, lines 23-25: acceleration, improvements of arithmetic operations; col. 3, lines 28-32: arithmetic operations utilized to generate cryptographic key(s); col. 3, lines 18-22: processor utilization for key generation)

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 6 - 12, 24 - 29, 31, 32, 47, 48, 53, 54, 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Gressel et al.** (US Patent No. 6,748,410) in view of **Stribaek et al.** (US Patent No. 7,181,484).

Regarding Claim 6, Gressel discloses the method as recited in claim 5, wherein said storing the high order portion of the generated result comprises storing the high order portion of the generated result into a register for use with execution of the subsequent single arithmetic instruction. (see Gressel col. 2, lines 4-9; col. 5, lines 58-67; col. 41, lines 20-23: register usage; col. 2, lines 31-37: multiplication, summing operations utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results) Gressel does not specifically disclose an extended carry register. And, Stribaek discloses wherein an extended carry register. (see Stribaek col. 5, lines 41-45: load value extended carry operations)

It would have been obvious to one of ordinary skill in the art to modify Gressel as taught by Stribaek to enable the capability for the usage of an extended carry register. One of ordinary skill in the art would have been motivated to employ the teachings of Stribaek in order to enable the capability for extended precision in arithmetic calculations due to extensive and increasing usage of public key cryptography. (see Stribaek col. 1, lines 61-67: “*... Public-key cryptosystems have been used extensively for user authentication and secure key exchange, while private-key cryptography has been used extensively to encrypt communication channels. As the use of public-key cryptosystems increases, it becomes desirable to increase the performance of extended-precision modular arithmetic calculations. ...*”)

Regarding Claim 7, Gressel discloses the method as recited in claim 6, further

comprising retrieving an indication of a current value of the register by executing another single arithmetic instruction that multiplies a third number by a fourth number and that implicitly adds current contents of the extended carry register to generate a second result that represents the third number multiplied by the fourth number summed with the current contents of the register. (see Gressel col. 2, lines 31-37: multiplication two values, summing two values utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results from previous multiplication) Gressel does not specifically disclose an extended carry register. And, Stribaek discloses wherein an extended carry register. (see Stribaek col. 5, lines 41-45: load value extended carry operations)

It would have been obvious to one of ordinary skill in the art to modify Gressel as taught by Stribaek to enable the capability for the usage of an extended carry register. One of ordinary skill in the art would have been motivated to employ the teachings of Stribaek in order to enable the capability for extended precision in arithmetic calculations due to extensive and increasing usage of public key cryptography. (see Stribaek col. 1, lines 61-67)

Regarding Claim 8, Gressel discloses the method as recited in claim 7, wherein a low order portion of the second result contains the indication of the current value of the register. (see Gressel col. 2, lines 31-37: arithmetic operations utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results) Gressel does not specifically disclose an extended carry register. And, Stribaek discloses wherein an

extended carry register. (see Stribaek col. 5, lines 41-45: load value extended carry operations)

It would have been obvious to one of ordinary skill in the art to modify Gressel as taught by Stribaek to enable the capability for the usage of an extended carry register. One of ordinary skill in the art would have been motivated to employ the teachings of Stribaek in order to enable the capability for extended precision in arithmetic calculations due to extensive and increasing usage of public key cryptography. (see Stribaek col. 1, lines 61-67)

Regarding Claim 9, Gressel discloses the method as recited in claim 7, wherein the third and fourth numbers are zero. (see Gressel col. 29, lines 43-49: representation of numbers)

Regarding Claim 10, Gressel discloses the method as recited in claim 6, further comprising loading the register with a predetermined value by executing another single arithmetic instruction that multiplies a third number by a fourth number and that implicitly adds a current value of the extended carry register, to generate a result that represents the third number multiplied by the fourth number summed with the current value of the register, thereby loading the register with the predetermined value. (see Gressel col. 2, lines 31-37: multiplication two values, summing two values utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results from previous multiplication) Gressel does not specifically disclose an extended carry register. And,

Stribaek discloses wherein an extended carry register. (see Stribaek col. 5, lines 41-45: load value extended carry operations)

It would have been obvious to one of ordinary skill in the art to modify Gressel as taught by Stribaek to enable the capability for the usage of an extended carry register. One of ordinary skill in the art would have been motivated to employ the teachings of Stribaek in order to enable the capability for extended precision in arithmetic calculations due to extensive and increasing usage of public key cryptography. (see Stribaek col. 1, lines 61-67)

Regarding Claim 11, Stribaek discloses the method as recited in claim 6, further comprising selecting one of a plurality of extended carry registers as the extended carry register. (see Stribaek col. 5, lines 41-45: extended carry operations)

It would have been obvious to one of ordinary skill in the art to modify Gressel as taught by Stribaek to enable the capability for the usage of an extended carry register. One of ordinary skill in the art would have been motivated to employ the teachings of Stribaek in order to enable the capability for extended precision in arithmetic calculations due to extensive and increasing usage of public key cryptography. (see Stribaek col. 1, lines 61-67)

Regarding Claim 12, Gressel discloses the method as recited in claim 6, further comprising accessing the register via at least one of a load instruction and a store instruction. (see Gressel col. 3, lines 28-32; col. 11, lines 7-11; col. 11, lines 40-49:

arithmetic operation or instructions) Gressel does not specifically disclose an extended carry register. And, Stribaek discloses wherein an extended carry register. (see Stribaek col. 5, lines 41-45: extended carry operations)

It would have been obvious to one of ordinary skill in the art to modify Gressel as taught by Stribaek to enable the capability for the usage of an extended carry register. One of ordinary skill in the art would have been motivated to employ the teachings of Stribaek in order to enable the capability for extended precision in arithmetic calculations due to extensive and increasing usage of public key cryptography. (see Stribaek col. 1, lines 61-67)

Regarding Claim 24, Gressel discloses the method as recited in claim 23 wherein said storing the high order portion of the generated result comprises storing the high order portion of the generated result into a register for use with execution of the subsequent arithmetic instruction. (see Gressel col. 3, lines 1-7; col. 53, lines 13-19; col. 53, lines 49-51: feedback of a previous operation into next operation) Gressel does not specifically disclose an extended carry register. However, Stribaek discloses wherein an extended carry register. (see Stribaek col. 5, lines 41-45: extended carry operations)

It would have been obvious to one of ordinary skill in the art to modify Gressel as taught by Stribaek to enable the capability for the usage of an extended carry register. One of ordinary skill in the art would have been motivated to employ the teachings of Stribaek in order to enable the capability for extended precision in arithmetic

calculations due to extensive and increasing usage of public key cryptography. (see Stribaek col. 1, lines 61-67)

Regarding Claim 25, Gressel discloses the method as recited in claim 24, further comprising retrieving an indication of a current value of the register by executing another single arithmetic instruction that multiplies a fourth number by a fifth number, that implicitly adds current contents of the register, and that adds a sixth number to generate a second result that represents the fourth number multiplied by the fifth number summed with the current contents of the register and the sixth number. (see Gressel col. 2, lines 31-37: multiplication two values, summing two values utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results from previous multiplication) Gressel does not specifically disclose an extended carry register. However, Stribaek discloses wherein an extended carry register. (see Stribaek col. 5, lines 41-45: extended carry operations)

It would have been obvious to one of ordinary skill in the art to modify Gressel as taught by Stribaek to enable the capability for the usage of an extended carry register. One of ordinary skill in the art would have been motivated to employ the teachings of Stribaek in order to enable the capability for extended precision in arithmetic calculations due to extensive and increasing usage of public key cryptography. (see Stribaek col. 1, lines 61-67)

Regarding Claim 26, Gressel discloses the method as recited in claim 25, wherein a low order portion of the second result contains the indication of the current value of the register. (see Gressel col. 2, lines 31-37: arithmetic operations utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results from previous operations) Gressel does not specifically disclose an extended carry register. However, Stribaek discloses wherein an extended carry register. (see Stribaek col. 5, lines 41-45: extended carry operations)

It would have been obvious to one of ordinary skill in the art to modify Gressel as taught by Stribaek to enable the capability for the usage of an extended carry register. One of ordinary skill in the art would have been motivated to employ the teachings of Stribaek in order to enable the capability for extended precision in arithmetic calculations due to extensive and increasing usage of public key cryptography. (see Stribaek col. 1, lines 61-67)

Regarding Claim 27, Gressel discloses the method as recited in claim 24, further comprising loading the register with a predetermined value by executing another single arithmetic instruction that multiplies a fourth number by a fifth number; and implicitly adds a current value of the register and adds a sixth number, to generate a result that represents the third number multiplied by the fourth number summed with the current value of the register and summed with the sixth number and to store it in the register, thereby loading the register with the predetermined value. (see Gressel col. 2, lines 31-37: multiplication two values, summing two values utilizing partial (i.e. bit operations,

any bit length, high order bits, low order bits) results from previous multiplication)

Gressel does not specifically disclose an extended carry register. However, Stribaek discloses wherein an extended carry register. (see Stribaek col. 5, lines 41-45: extended carry operations)

It would have been obvious to one of ordinary skill in the art to modify Gressel as taught by Stribaek to enable the capability for the usage of an extended carry register. One of ordinary skill in the art would have been motivated to employ the teachings of Stribaek in order to enable the capability for extended precision in arithmetic calculations due to extensive and increasing usage of public key cryptography. (see Stribaek col. 1, lines 61-67)

Regarding Claim 28, Stribaek discloses the method as recited in claim 24, further comprising selecting one of a plurality of extended carry registers as the extended carry register. (see Stribaek col. 5, lines 41-45: extended carry operations)

It would have been obvious to one of ordinary skill in the art to modify Gressel as taught by Stribaek to enable the capability for the usage of an extended carry register. One of ordinary skill in the art would have been motivated to employ the teachings of Stribaek in order to enable the capability for extended precision in arithmetic calculations due to extensive and increasing usage of public key cryptography. (see Stribaek col. 1, lines 61-67)

Regarding Claim 29, Stribaek discloses the method as recited in claim 24, further

comprising accessing the extended carry register via at least one of a load instruction and a store instruction. (see Stribaek col. 5, lines 41-45: extended carry operations)

It would have been obvious to one of ordinary skill in the art to modify Gressel as taught by Stribaek to enable the capability for the usage of an extended carry register. One of ordinary skill in the art would have been motivated to employ the teachings of Stribaek in order to enable the capability for extended precision in arithmetic calculations due to extensive and increasing usage of public key cryptography. (see Stribaek col. 1, lines 61-67)

Regarding Claim 31, Gressel discloses the method as recited in claim 30 further comprising accessing a register storing the second number via at least one of a load instruction and a store instruction. (see Gressel col. 3, lines 28-32; col. 11, lines 7-11; col. 11, lines 40-49: arithmetic operation or instructions) Gressel does not specifically disclose a special register. However, Stribaek discloses wherein a special register. (see Stribaek col. 5, lines 41-45: special register (extended carry register))

It would have been obvious to one of ordinary skill in the art to modify Gressel as taught by Stribaek to enable the capability for the usage of a special register (an extended carry register). One of ordinary skill in the art would have been motivated to employ the teachings of Stribaek in order to enable the capability for extended precision in arithmetic calculations due to extensive and increasing usage of public key cryptography. (see Stribaek col. 1, lines 61-67)

Regarding Claim 32, Gressel discloses the method as recited in claim 18 further comprising accessing a special register storing the second number via at least one of a load instruction and a store instruction. (see Gressel col. 3, lines 28-32; col. 11, lines 7-11; col. 11, lines 40-49: arithmetic operation or instructions) Gressel does not specifically disclose a special register. However, Stribaek discloses wherein a special register. (see Stribaek col. 5, lines 41-45: extended carry operations; col. 7, lines 31-37; col. 9, lines 10-14: carry-save adder)

It would have been obvious to one of ordinary skill in the art to modify Gressel as taught by Stribaek to enable the capability for the usage of a special register (an extended carry register). One of ordinary skill in the art would have been motivated to employ the teachings of Stribaek in order to enable the capability for extended precision in arithmetic calculations due to extensive and increasing usage of public key cryptography. (see Stribaek col. 1, lines 61-67)

Regarding Claim 47, Gressel discloses the processor as recited in claim 45, wherein the register has an associated dirty bit indicating whether contents of the register need to be saved on a context switch. (see Gressel col. 24, lines 4-10: switch based on context of data) Gressel does not specifically disclose an extended carry register. However, Stribaek discloses wherein an extended carry register. (see Stribaek col. 5, lines 41-45: extended carry operations)

It would have been obvious to one of ordinary skill in the art to modify Gressel as taught by Stribaek to enable the capability for the usage of an extended carry register.

One of ordinary skill in the art would have been motivated to employ the teachings of Stribaek in order to enable the capability for extended precision in arithmetic calculations due to extensive and increasing usage of public key cryptography. (see Stribaek col. 1, lines 61-67)

Regarding Claim 48, Stribaek discloses the processor as recited in claim 43, wherein the extended carry register is a special register. (see Stribaek col. 5, lines 41-45: extended carry register)

It would have been obvious to one of ordinary skill in the art to modify Gressel as taught by Stribaek to enable the capability for the usage of a special register (an extended carry register). One of ordinary skill in the art would have been motivated to employ the teachings of Stribaek in order to enable the capability for extended precision in arithmetic calculations due to extensive and increasing usage of public key cryptography. (see Stribaek col. 1, lines 61-67)

Regarding Claim 53, Gressel discloses the processor as recited in claim 50, wherein the processor is configured to store the high order portion of the generated result into a register. (see Gressel col. 2, lines 31-37: arithmetic operations utilizing partial (i.e. bit operations, any bit length, high order bits, low order bits) results) Gressel does not specifically disclose an extended carry register. However, Stribaek discloses wherein an extended carry register. (see Stribaek col. 5, lines 41-45: extended carry register)

It would have been obvious to one of ordinary skill in the art to modify Gressel as taught by Stribaek to enable the capability for the usage of an extended carry register. One of ordinary skill in the art would have been motivated to employ the teachings of Stribaek in order to enable the capability for extended precision in arithmetic calculations due to extensive and increasing usage of public key cryptography. (see Stribaek col. 1, lines 61-67)

Regarding Claim 54, Gressel discloses the processor as recited in claim 50, wherein the register is a special register accessible by the processor via at least one of load instruction and store instructions. (see Gressel col. 3, lines 28-32; col. 11, lines 7-11; col. 11, lines 40-49: arithmetic operations or instructions) Gressel does not specifically disclose an extended carry register. However, Stribaek discloses wherein an extended carry register. (see Stribaek col. 5, lines 41-45: extended carry register)

It would have been obvious to one of ordinary skill in the art to modify Gressel as taught by Stribaek to enable the capability for the usage of an extended carry register. One of ordinary skill in the art would have been motivated to employ the teachings of Stribaek in order to enable the capability for extended precision in arithmetic calculations due to extensive and increasing usage of public key cryptography. (see Stribaek col. 1, lines 61-67)

Regarding Claim 55, Gressel discloses the processor as recited in claim 50, wherein the register has an associated dirty bit indicating whether contents of the register need

to be saved on a context switch. (see Gressel col. 24, lines 4-10: switch based on context of data) Gressel does not specifically disclose an extended carry register. However, Stribaek discloses wherein an extended carry register. (see Stribaek col. 5, lines 41-45: extended carry register)

It would have been obvious to one of ordinary skill in the art to modify Gressel as taught by Stribaek to enable the capability for the usage of an extended carry register. One of ordinary skill in the art would have been motivated to employ the teachings of Stribaek in order to enable the capability for extended precision in arithmetic calculations due to extensive and increasing usage of public key cryptography. (see Stribaek col. 1, lines 61-67)

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carlton V. Johnson whose telephone number is 571-270-1032. The examiner can normally be reached on Monday thru Friday , 8:00 - 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nasser Moazzami can be reached on 571-272-4195. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

C.J.
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September 4, 2007

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9/17/07